CLAIM LISTING

1. (Currently amended) A substrate with a via and pad structure for connecting a surface mount component to conductive layers of the substrate, wherein the surface mount component includes a package having an upper surface with solderable terminal sides and a terminal end, comprising:

a substrate;

a plated via connected to the conductive layers;

a solder mask surrounding the plated via; and

a conductive pad with a conductive trace connected to the plated via, wherein the solder mask exposes a part of the conductive pad that extends beyond the solderable terminal sides of the surface mount component to increase solder formation [at] between the conductive pad and the solderable terminal sides.

2. (Currently amended) The substrate with the via and pad structure of claim 1, wherein the solder mask covers and reduces solder formation at the terminal end of the surface mount component.

3. (Currently amended) The substrate with the via and pad structure of claim 2, wherein the conductive pad includes a first arm and a second arm that extend beyond the solderable terminal sides of the surface mount component.

4. (Original) The substrate with the via and pad structure of claim 3, wherein the first arm and the second arm are symmetrically disposed on the substrate with respect to the plated via.

5. (Original) The substrate with the via and pad structure of claim 2, wherein the conductive pad includes a first arm, a second arm, and a body.

6. (Original) The substrate with the via and pad structure of claim 5, wherein the first arm and the second arm are symmetrically disposed on the substrate with respect to the plated via.

7. (Original) The substrate with the via and pad structure of claim 2, wherein the conductive pad includes a T-shirt shaped structure.

8. (Original) The substrate with the via and pad structure of claim 7, wherein the T-shirt shaped structure is symmetrically disposed on the substrate with respect to the plated via.

9. (Original) The substrate with the via and pad structure of claim 2, wherein the solder mask is keyhole shaped.

10. (Original) The substrate with the via and pad structure of claim 2, wherein the solder mask covers the substrate partially or entirely except the conductive pad and the plated via.

11. (Currently amended) The substrate with the via and pad structure of claim 2, further comprising a surface mount component electrically connected to the conductive pad through solder joint(s), wherein the solder joints have a greater volume at the solderable terminal sides than at the terminal end of the surface mount component.

12. (Original) The substrate with the via and pad structure of claim 2, wherein the substrate is part of a printed circuit board.

13. (Currently amended) The substrate with the via and pad structure of claim 2, wherein the substrate is part of a BGA package footprint.

14. (Currently amended) A substrate with a plurality of via and pad structures for connecting a surface mount component to conductive layers of the substrate, wherein the surface mount component includes a package having an upper surface with first solderable terminal sides and a first terminal end and second solderable terminal sides and a second terminal end, comprising:

a substrate;

a first plated via connected to the conductive layers;

a first solder mask surrounding the first plated via;

a second plated via connected to an associated conductive layer;

a second solder mask surrounding the second plated via;

a first conductive pad with a conductive trace connected to the first plated via, wherein the first conductive pad includes a portion that is exposed to solder and extends beyond the first solderable terminal sides of the surface mount component to increase solder formation along the first solderable terminal sides; and

a second conductive pad with a conductive trace connected to the second plated via, wherein the second conductive pad includes a portion that is exposed to solder and extends beyond the second solderable terminal sides of the surface mount component to increase solder formation along the second solderable terminal sides.

15. (Currently amended) The substrate with the plurality of via and pad structures of claim 14, wherein the first solder mask covers and reduces solder formation at [one] the first terminal end of the surface mount component and the second solder mask covers and reduces solder formation at the [other] second terminal end of the surface mount component.

16. (Previously presented) The substrate with the plurality of via and pad structures of claim 15, wherein each of the first and second conductive pads include a first arm and a second arm.

17. (Original) The substrate with the plurality of via and pad structures of claim 16, wherein each of the first and second conductive pads is symmetric to the first plated via and the second plated vias, respectively.

18. (Original) The substrate with the plurality of via and pad structures of claim 15, wherein the first and second conductive pads include a first arm, a second arm, and a body.

19. (Original) The substrate with the plurality of via and pad structures of claim 18, wherein each of the first and second conductive pads is symmetric to the first plated via and the second plated vias, respectively.

20. (Original) The substrate with the plurality of via and pad structures of claim 15, wherein each of the first and second conductive pads include a T-shirt shaped structure.

21. (Original) The substrate with the plurality of via and pad structures of claim 20, wherein each of the T-shirt shaped structures is symmetric to the first and second plated vias, respectively.

22. (Original) The substrate with the plurality of via and pad structures of claim 15, wherein each of the first and second solder masks is a ring surrounding the first and second plated vias, respectively.

23. (Original) The substrate with the plurality of via and pad structures of claim 15, wherein each of the first and second solder masks is a keyhole shape and surrounds the first and second plated vias, respectively.

24. (Original) The substrate with the plurality of via and pad structures of claim 15, wherein each of the first and second solder masks cover the substrate

partially or entirely except the first and second conductive pads and the first and second plated vias.

25. (Currently amended) The substrate with the plurality of via and pad structures of claim 15, further comprising a surface mount component electrically connected to the first and second conductive pads through solder joint(s), wherein the solder joint(s) have a greater volume at each of the solderable terminal sides than at each terminal end of the surface mount component.

26. (Currently amended) The substrate with the plurality of via and pad structures of claim 15, wherein the separation along the substrate between the first and second solder masks defines the length of the surface mount component to be soldered.

27. (Original) The substrate with the plurality of via and pad structures of claim 15, wherein the substrate is part of a printed circuit board.

28. (Currently amended) The substrate with the plurality of via and pad structures of claim 15, wherein the substrate is part of a BGA package footprint.

29. (Original) The substrate with the via and pad structure of claim 2, wherein solder mask is a ring surrounding the plated via.

30. (Withdrawn) A method of reducing solder wicking on a substrate with associated conductive layers, comprising:

(a) forming a via and pad structure;

(b) masking around the plated via to reduce solder formation at the plated via;

(c) placing a component having terminal sides and a terminal end on the conductive pad;

(d) extending the conductive pad beyond the terminal sides of the component to increase solder formation along the terminal sides; and

(e) soldering the component to the conductive pad.

31. (Withdrawn) The method of claim 30, further comprising repeating steps (a) through (e) for a plurality of via and pad structures.

32. (Withdrawn) The method of claim 30, wherein the conductive pad is a T-shirt shaped structure.

33. (Withdrawn) The method of claim 31, wherein the masking around plated via is accomplished by a keyhole shaped structure.

34. (Original) The substrate with the plurality of via and pad structures of claim 14, wherein the first conductive pad extends beyond the terminal side of the component a maximum distance that reduces solder wicking without generating electrical shorts between the first conductive pad and an adjacent plated via.

35. (Withdrawn) A computer implemented method for calculating the maximum distance of a conductive pad extending beyond the terminal side of a component, wherein the component is placed diagonally in an array of four plated vias, comprising:

(a) storing L1 representing the center-to-center distance of a first plated via and a second plated via;

(b) storing L3 representing the length and L4 the width of the component;

(c) storing L5 representing the length of the conductive pad extending beyond the terminal side;

(d) storing R representing an outer radius of a first plated via;

(e) storing X representing the minimum distance between the first plated via and the conductive pad;

(f) calculating L2, representing the center-to-center distance between the first plated via and a third plated via, by dividing L1 by sin 45°;

(g) calculating L8, representing the distance from the center of the first plated via to the side of the component, by subtracting L4 from L2 and dividing by two;

(h) calculating L7, representing half the distance between the conductive pad and an opposite conductive pad, by dividing L3 by two and subtracting L5;

(i) calculating L11 by summing R and X;

(j) calculating L9 by taking the square root of the difference of the square of L11 and the square of L7; and

(k) calculating L10 by subtracting L9 from L8, wherein L10 is the maximum distance of the conductive pad extending beyond the terminal side of the component.